IN THE CLAIMS:

Please cancel claims 2, 12 and 14 without prejudice or disclaimer as to the subject matter recited therein.

Please amend the claims as follows.

1. (Currently Amended) A central processing unit (CPU) comprising:

a register file including a standard register set and an extended register set, wherein the standard register set comprises a plurality of standard registers, and wherein the extended register set comprises a plurality of extended registers; and

an execution core coupled to the register file and to receive a signal indicating an operating mode of the CPU, wherein the execution core is configured to fetch and execute instructions, and wherein the execution core is configured to respond to an instruction by accessing at least one extended register if the signal indicates the CPU is operating in an extended register mode and the instruction includes a prefix portion including information needed to access the at least one extended register;

wherein the number of standard registers is less than or equal to a number of general purpose registers defined by a CPU architecture, and wherein the number of extended registers is greater than the number of general purpose registers defined by the CPU architecture.

2. Cancelled.

3. (Original) The CPU as recited in claim 1, wherein the instruction absent the prefix portion includes register identification information sufficient to identify a selected one of the

standard registers, and wherein the prefix portion of the instruction includes additional register identification information needed to identify a selected one of the extended registers.

4. (Original) The CPU as recited in claim 1, wherein the encoding of the instruction, including the prefix portion, identifies the at least one extended register accessed by the execution core.

5. (Original) The CPU as recited in claim 1, wherein the standard register set comprises eight 32-bit general purpose registers defined by the x86 architecture.

6. (Original) The CPU as recited in claim 5, wherein the eight 32-bit general purpose registers include the EAX, EBX, ECX, EDX, ESP, EBP, ESI, and EDI registers.

7. (Original) The CPU as recited in claim 5, wherein the standard register set comprises eight 32-bit general purpose registers defined by the x86 architecture, and wherein the extended register set includes the eight 32-bit general purpose registers of the standard register set and eight additional 32-bit registers not defined by the x86 architecture.

8. (Original) The CPU as recited in claim 1, wherein the execution core is configured to fetch and execute variable-length x86 instructions.

9. (Original) The CPU as recited in claim 1, wherein the prefix portion comprises an extended register prefix byte, and wherein the extended register prefix byte comprises an extended register key field, and wherein the contents of the extended register key field indicates whether or not the extended register prefix byte includes the information needed to access the at least one extended register.

10. (Currently Amended) The CPU as recited in claim [[1]] 9, wherein the extended register prefix byte includes the information needed to access the at least one extended register only when the extended register key field contains a predetermined extended register key value.

11. (Original) The CPU as recited in claim 1, further comprising:

a control register for storing information indicating whether or not the extended register mode is globally enabled;

a flags register for storing information indicating whether or not the extended register mode is enabled by a current process; and

generating means for generating the signal indicating the operating mode of the CPU, wherein the signal indicates the CPU is operating in the extended register mode if the extended register mode is globally enabled and enabled by the current process.

12. Cancelled.

13. (Currently Amended) A central processing unit (CPU) comprising:

a register file including a standard register set and an extended register set, wherein the standard register set comprises a plurality of 32-bit general purpose registers defined by the x86 architecture, and wherein the extended register set comprises a plurality of extended registers, and wherein the number of extended registers is greater than the number of general purpose registers defined by the x86 architecture; and

an execution core coupled to the register file and to receive a signal indicating an operating mode of the CPU, wherein the execution core is configured to fetch and execute variable-length x86 instructions, and wherein the execution core is configured to respond to an instruction by accessing at least one extended register if the signal indicates the CPU is operating in an extended register mode and the instruction includes an extended register prefix byte including information needed to access the at least one extended register;

wherein the instruction absent the extended register prefix byte includes register identification information sufficient to identify a selected one of the standard registers, and wherein the extended register prefix byte includes additional register identification information needed to identify a selected one of the extended registers.

14. Cancelled.

15. (Original) The CPU as recited in claim 13, wherein the encoding of the instruction, including the extended register prefix byte, identifies the at least one extended register accessed by the execution core.

16. (Original) The CPU as recited in claim 13, wherein the standard register set comprises the EAX, EBX, ECX, EDX, ESP, EBP, ESI, and EDI registers defined by the x86 architecture.

17. (Original) The CPU as recited in claim 13, wherein the standard register set comprises eight 32-bit general purpose registers defined by the x86 architecture, and wherein the extended register set includes the eight 32-bit general purpose registers of the standard register set and eight additional 32-bit registers not defined by the x86 architecture.

18. (Original) The CPU as recited in claim 13, wherein the extended register prefix byte comprises an extended register key field, and wherein the contents of the extended register key field indicates whether or not the extended register prefix byte includes the information needed to access the at least one extended register.

19. (Original) The CPU as recited in claim 18, wherein the extended register prefix byte includes the information needed to access the at least one extended register only when the extended register key field contains a predetermined extended register key value.

20. (Original) The CPU as recited in claim 13, further comprising:

a control register for storing information indicating whether or not the extended register mode is globally enabled;

a flags register for storing information indicating whether or not the extended register mode is enabled by a current process; and

generating means for generating the signal indicating the operating mode of the CPU, wherein the signal indicates the CPU is operating in the extended register mode if the extended register mode is globally enabled and enabled by the current process.

21. (Original) A central processing unit (CPU) comprising:

a register file including a standard register set and an extended register set, wherein the standard register set comprises a plurality of general purpose registers defined by a CPU architecture, and wherein the extended register set comprises a plurality of extended registers, and wherein the number of extended registers is greater than the number of general purpose registers defined by the CPU architecture, and wherein a width of the extended registers is greater than a width of the general purpose registers defined by the CPU architecture; and

an execution core coupled to the register file and to receive the signal indicating the operating mode of the CPU, wherein the execution core is configured to fetch and execute instructions, and wherein the execution core is configured to respond to an instruction by accessing the entire contents of at least one extended register if: (i) the signal indicates the CPU is operating in an extended register mode, (ii) the instruction includes a prefix portion including information needed to access the at least one extended register, and (iii) the prefix portion includes an indication that the entire contents of the least one extended register is to be accessed.

22. (Original) The CPU as recited in claim 21, wherein the CPU architecture is the x86 architecture, and wherein the width of the general purpose registers is 32 bits, and wherein the width of the extended registers is 64 bits.

23. (Original) The CPU as recited in claim 22, wherein the standard register set includes the EAX, EBX, ECX, EDX, ESP, EBP, ESI, and EDI registers defined by the x86 architecture.

24. (Original) The CPU as recited in claim 23, wherein the standard register set is a subset of the extended register set, and wherein the standard registers form lower ordered portions of extended registers.

25. (Original) The CPU as recited in claim 21, wherein the instruction absent the prefix portion includes register identification information sufficient to identify a selected one of the standard registers, and wherein the prefix portion of the instruction includes additional register identification information needed to identify a selected one of the extended registers.

26. (Original) The CPU as recited in claim 21, wherein the encoding of the instruction, including the prefix portion, identifies the at least one extended register accessed by the execution core.

27. (Original) The CPU as recited in claim 21, wherein the execution core is configured to fetch and execute variable-length x86 instructions.

28. (Original) The CPU as recited in claim 21, wherein the prefix portion comprises an extended register prefix byte, and wherein the extended register prefix byte comprises: (i) an extended register key field, wherein the contents of the extended register key field indicates whether or not the extended register prefix byte includes the information needed to access the at least one extended register, and (ii) an operand size override bit, wherein the value of the operand size override bit indicates whether or not the entire contents of the least one extended register is to be accessed.

29. (Original) The CPU as recited in claim 21, wherein the extended register prefix byte includes the information needed to access the at least one extended register and the indication that the entire contents of the least one extended register is to be accessed only when the extended register key field contains a predetermined extended register key value.

30. (Original) The CPU as recited in claim 21, further comprising:

a control register for storing information indicating whether or not the extended register mode is globally enabled;

a flags register for storing information indicating whether or not the extended register mode is enabled by a current process; and

generating means for generating the signal indicating the operating mode of the CPU, wherein the signal indicates the CPU is operating in the extended register mode if the extended register mode is globally enabled and enabled by the current process.

31. (New) A central processing unit (CPU) comprising:

a register file including a standard register set and an extended register set, wherein the standard register set comprises a plurality of standard registers, and wherein the extended register set comprises a plurality of extended registers; and

an execution core coupled to the register file and to receive a signal indicating an operating mode of the CPU, wherein the execution core is configured to fetch and execute instructions, and wherein the execution core is configured to respond to an instruction by accessing at least one extended register if the signal indicates the CPU is operating in an extended register mode and the instruction includes a prefix portion including information needed to access the at least one extended register;

wherein the instruction absent the prefix portion includes register identification information sufficient to identify a selected one of the standard registers, and wherein the prefix portion of the instruction includes additional register identification information needed to identify a selected one of the extended registers.

32. (New) The CPU as recited in claim 31, wherein the standard register set comprises eight 32-bit general purpose registers defined by the x86 architecture.

33. (New) A central processing unit (CPU) comprising:

a register file including a standard register set and an extended register set, wherein the standard register set comprises a plurality of standard registers, and wherein the extended register set comprises a plurality of extended registers; and

an execution core coupled to the register file and to receive a signal indicating an operating mode of the CPU, wherein the execution core is configured to fetch and execute instructions, and wherein the execution core is configured to respond to an instruction by accessing at least one extended register if the signal indicates the CPU is operating in an extended register mode and the instruction includes a prefix portion including information needed to access the at least one extended register;

wherein the standard register set comprises eight 32-bit general purpose registers defined by the x86 architecture;

wherein the eight 32-bit general purpose registers include the EAX, EBX, ECX, EDX, ESP, EBP, ESI, and EDI registers; and

wherein the extended register set includes the eight 32-bit general purpose registers of the standard register set and eight additional 32-bit registers not defined by the x86 architecture.

34. (New) The CPU as recited in claim 33, wherein the instruction absent the prefix portion includes register identification information sufficient to identify a selected one of the standard registers, and wherein the prefix portion of the instruction includes additional register identification information needed to identify a selected one of the extended registers.

35. (New) A central processing unit (CPU) comprising:

a register file including a standard register set and an extended register set, wherein the standard register set comprises a plurality of standard registers, and wherein the extended register set comprises a plurality of extended registers; and

an execution core coupled to the register file and to receive a signal indicating an operating mode of the CPU, wherein the execution core is configured to fetch and execute instructions, and wherein the execution core is configured to respond to an instruction by accessing at least one extended register if the signal indicates the CPU is operating in an extended register mode and the instruction includes a prefix portion including information needed to access the at least one extended register;

wherein the prefix portion comprises an extended register prefix byte, and wherein the extended register prefix byte comprises an extended register key field, and wherein the contents of the extended register key field indicates whether or not the extended register prefix byte includes the information needed to access the at least one extended register.

36. (New) The CPU as recited in claim 35, wherein the extended register prefix byte includes the information needed to access the at least one extended register only when the extended register key field contains a predetermined extended register key value.

37. (New) A central processing unit (CPU) comprising:

a register file including a standard register set and an extended register set, wherein the standard register set comprises a plurality of standard registers, and wherein the extended register set comprises a plurality of extended registers;

an execution core coupled to the register file and to receive a signal indicating an operating mode of the CPU, wherein the execution core is configured to fetch and execute instructions, and wherein the execution core is configured to respond to an instruction by accessing at least one extended register if the signal indicates the CPU is operating in an extended register mode and the instruction includes a prefix portion including information needed to access the at least one extended register;

a control register for storing information indicating whether or not the extended register mode is globally enabled;

a flags register for storing information indicating whether or not the extended register mode is enabled by a current process; and

generating means for generating the signal indicating the operating mode of the CPU, wherein the signal indicates the CPU is operating in the extended register mode if the extended register mode is globally enabled and enabled by the current process.

38. (New) A central processing unit (CPU) comprising:

a register file including a standard register set and an extended register set, wherein the standard register set comprises a plurality of 32-bit general purpose registers defined by the x86 architecture, and wherein the extended register set comprises a plurality of extended registers, and wherein the number of extended registers is greater than the number of general purpose registers defined by the x86 architecture; and

an execution core coupled to the register file and to receive a signal indicating an operating mode of the CPU, wherein the execution core is configured to fetch and execute variable-length x86 instructions, and wherein the execution core is configured to respond to an instruction by accessing at least one extended register if the signal indicates the CPU is operating in an extended register mode and the instruction includes an extended register prefix byte including information needed to access the at least one extended register;

wherein the standard register set comprises eight 32-bit general purpose registers defined by the x86 architecture, and wherein the extended register set includes the eight 32-bit general purpose registers of the standard register set and eight additional 32-bit registers not defined by the x86 architecture.

39. (New) The CPU as recited in claim 38, wherein the instruction absent the extended register prefix byte includes register identification information sufficient to identify a selected one of the standard registers, and wherein the extended register prefix byte includes additional register identification information needed to identify a selected one of the extended registers.

40. (New) A central processing unit (CPU) comprising:

a register file including a standard register set and an extended register set, wherein the standard register set comprises a plurality of 32-bit general purpose registers defined by the x86 architecture, and wherein the extended register set comprises a

plurality of extended registers, and wherein the number of extended registers is greater than the number of general purpose registers defined by the x86 architecture; and

an execution core coupled to the register file and to receive a signal indicating an operating mode of the CPU, wherein the execution core is configured to fetch and execute variable-length x86 instructions, and wherein the execution core is configured to respond to an instruction by accessing at least one extended register if the signal indicates the CPU is operating in an extended register mode and the instruction includes an extended register prefix byte including information needed to access the at least one extended register;

wherein the extended register prefix byte comprises an extended register key field, and wherein the contents of the extended register key field indicates whether or not the extended register prefix byte includes the information needed to access the at least one extended register.

41. (New) The CPU as recited in claim 40, wherein the extended register prefix byte includes the information needed to access the at least one extended register only when the extended register key field contains a predetermined extended register key value.

42. A central processing unit (CPU) comprising:

a register file including a standard register set and an extended register set, wherein the standard register set comprises a plurality of 32-bit general purpose registers defined by the x86 architecture, and wherein the extended register set comprises a plurality of extended registers, and wherein the number of extended registers is greater than the number of general purpose registers defined by the x86 architecture;

an execution core coupled to the register file and to receive a signal indicating an operating mode of the CPU, wherein the execution core is configured to fetch and execute variable-length x86 instructions, and wherein the execution core is configured to respond to an instruction by accessing at least one extended register if the signal indicates the CPU is operating in an extended register mode and the instruction includes an extended register prefix byte including information needed to access the at least one extended register;

a control register for storing information indicating whether or not the extended register mode is globally enabled;

a flags register for storing information indicating whether or not the extended register mode is enabled by a current process; and

generating means for generating the signal indicating the operating mode of the CPU, wherein the signal indicates the CPU is operating in the extended register mode if the extended register mode is globally enabled and enabled by the current process.